IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A semiconductor memory device having a SRAM in which a memory cell comprises a pair of transmission transistors and a flip-flop circuit containing a pair of driver transistors and a pair of load transistors, wherein:

a first interconnection formed from a first electrical conductor which is set on a semiconductor substrate, constitutes respective gate electrodes of said drive transistors, load transistors and transmission transistors;

a second interconnection including a second electrical conductor, which is formed within a first trench that is set in a first insulating film lying on said semiconductor substrate, constitutes one of a pair of local interconnections cross-coupling a pair of input/out terminals in said flip-flop circuit;

a third interconnection which is formed on a second insulating film lying on a region including the top surface of said second interconnection, constitutes the other one of said pair of local interconnections; and

either said second interconnection or said third interconnection has a buried conductive section which is formed to fill up the inside of said trench,

said second electrical conductor being disposed so as to come in physical contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first interconnection A, the gate electrode being in common to said first driver transistor; and

a first interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors.

2. (Original) A semiconductor memory device according to Claim 1, wherein:

said second interconnection and said third interconnection have an overlapping section separated by said second insulating film; and

said second interconnection and said third interconnection, together with said second insulating film lying therebetween, constitute a capacitor element.

3. (Previously Presented) A semiconductor memory device according to Claim 1, wherein:

said third interconnection is in contact with

a contact section connected to said first interconnection A;

a contact section connected to a drain region of said second driver transistor; and

a contact section connected to a drain region of said second load transistor.

4. (Currently Amended) A semiconductor memory device having a SRAM in which a memory cell comprises a pair of transmission transistors and a flip-flop circuit containing a pair of driver transistors and a pair of load transistors, wherein:

a first conductive film interconnection formed from a first conductive film which is set on a semiconductor substrate, constitutes respective gate electrodes of said driver transistors, load transistors and transmission transistors;

an inlaid interconnection set in a first insulating film lying on said semiconductor substrate, constitutes one of a pair of local interconnections cross-coupling a pair of input/output terminals in said flip-flop circuit; and

a second conductive film interconnection formed from a second conductive film which is set on a second insulating film lying on said first insulating film, constitutes the other one of said pair of local interconnections,

said inlaid interconnection being disposed so as to come in physical contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first conductive film interconnection A, the gate electrode being in common to said first driver transistor, and

a first conductive film interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors.

5. (Original) A semiconductor memory device according to Claim 4, wherein

said second conductive film interconnection is disposed so as to overlap at least a portion of a top surface of said inlaid interconnection, with said second insulating film lying therebetween; and

said inlaid interconnection and said second conductive film interconnection, together with said second insulating film lying therebetween, constitute a capacitor element.

6. (Original) A semiconductor memory device according to Claim 5; wherein

said second conductive film interconnection is disposed so as to cover at least a portion of a lateral face of said inlaid interconnection, with said second insulating film placed therebetween; and

said inlaid interconnection and said second conductive film interconnection, together with said second insulating film lying therebetween, constitute a capacitor element.

7. (Previously Presented) A semiconductor memory device according to Claim 4, wherein:

said second conductive film interconnection is in contact with

a contact section to reach said first conductive film interconnection A;

a contact section to reach a drain region of said second driver transistor; and

a contact section to reach a drain region of said second load transistor.

8. (Original) A semiconductor memory device according to Claim 7, wherein said first conductive film interconnection B branches off between the drain region of said second driver transistor and the drain region of said second load transistor, and this branched section of interconnection comes into contact with said inlaid interconnection.

9. (Original) A semiconductor memory device according to Claim 8, wherein a contact region between said branched section of interconnection and said inlaid interconnection contains a point that is, seen from the substrate top surface, equidistant from any among a group of said contact section to reach the first conductive film interconnection A, said contact section to reach the drain region of the second driver transistor, and said contact section to reach the drain region of the second load transistor.

10. (Previously Presented) A semiconductor memory device according to Claim 1, wherein:

said second interconnection comprises said buried conductive section having at least said second electrical conductor and a stacked electrode which is set on said buried conductive section,

said second insulating film covers said stacked electrode; and

said third interconnection is disposed on said second insulating film so as to overlap, at least, a portion of a top surface and a portion of a lateral face of said stacked electrode, and said stacked electrode and said third interconnection, together with said second insulating film lying therebetween, constitute a capacitor element.

11. (Previously Presented) A semiconductor memory device according to Claim 1, wherein:

said device further comprises a second trench which is formed in a third insulating film lying on said first insulating film;

said second interconnection comprises said buried conductive section having at least said second electrical conductor and a third electrical conductor which covers an inner side surface and a bottom surface of said second trench and has a first hollow in said second trench, said third electrical conductor contacting with an upper surface of said buried conductive section in the bottom of said second trench;

said second insulating film is formed on said third electrical conductor and has a second hollow in said first hollow;

said third interconnection comprises a buried electrode which fills up said second hollow; and

said buried electrode and said third electrical conductor, together with said second insulating film lying therebetween, constitute a capacitor element.

12. (Original) A semiconductor memory device according to Claim 1, wherein:

said second electrical conductor covers an inner side surface and a bottom surface of said first trench and has a first hollow in said first trench;

said second insulating film is formed on said second electrical conductor and has a second hollow in said first hollow;

said third interconnection comprises said buried conductive section which fills up said second hollow; and

said second electrical conductor and said buried conductive section, together with said second insulating film lying therebetween, constitute a capacitor element.

13. (Previously Presented) A semiconductor memory device according to Claim 1, wherein a refractory metal silicide layer is formed on the surface of every gate electrode, source region and drain region of said pair of driver transistors, said pair of load transistors and said pair of transmission transistors.

14.-21. (Cancelled).

22. (New) A Static Random Access Memory (SRAM) cell, comprising:

a first diffusion region formed on a semiconductor substrate;

a second diffusion region formed on said semiconductor substrate;

a first conductive layer formed over said semiconductor substrate;

an interlayer insulating film formed on said semiconductor substrate, said interlayer insulating film having an opening which exposes said first and second diffusion layers and said first conductive layer;

a second conductive layer formed in said opening;

a dielectric layer formed on said second conductive layer; and

a third conductive layer formed on said dielectric layer, whereby a capacitor is formed by said second and third conductive layers and said dielectric layer.

23. (New) The SRAM cell as claimed in claim 22, said cell further comprising:

a first load transistor which has source and drain regions, one of which corresponds to said first diffusion region; and

a first drive transistor which has source and drain regions, one of which corresponds to said second diffusion region.

24. (New) The SRAM cell as claimed in claim 23, said cell further comprising:

a second load transistor and a second drive transistor, each of said second load transistor and said second drive transistor having a gate electrode;

wherein said first conductive layer has a "T" shape having two branches, one of said branches corresponding to said second load transistor and the other of said branches corresponding to said second drive transistor.

25. (New) The SRAM cell as claimed in claim 24, wherein a first contact is connected between said third conductive layer and a gate electrode of said first load transistor and of said first drive transistor, a second contact is connected between said third conductive layer and said second load transistor, and a third contact is connected between said third conductive layer and said second drive transistor.

26. (New) The SRAM cell as claimed in claim 25, wherein said gate electrode, said branches and said second conductive layer are arranged in parallel with one another.

27. (New) The SRAM cell as claimed in claim 22, wherein a top surface of said second conductive layer is higher than that of said interlayer insulating film.

28. (New) The SRAM cell as claimed in claim 27, wherein said dielectric layer is formed on facing side surfaces of said second conductive layer.

29. (New) The SRAM cell as claimed in claim 28, wherein said dielectric layer is formed on a single side of said facing side surfaces of said second conductive layer.

30. (New) The SRAM cell as claimed in claim 22, wherein a top surface of said second conductive layer is lower than that of said interlayer insulating film.

31. (New) The SRAM cell as claimed in claim 22, wherein said first conductive layer is formed on an element isolation layer on said semiconductor substrate.